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Question Paper Code : 70429

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2021.

Third Semester

Electronics and Communication Engineering

EC 6304 — ELECTRONIC CIRCUITS — I

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List out the three stability factor.

2. Find the collector and base current of circuit given in fig Q.2 hfe = 80, $V_{BE(ON)}$ = 0.7 V.

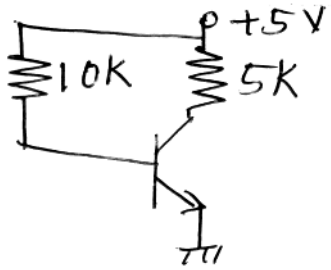

Fig. Q.2

3. What is an ac load line?

4. Draw the small-signal ac equivalent circuit of the BJT.

5. Calculate the output resistance of a source-follower circuit Given that $R_s = 0.75k\Omega$, $r_o = 12.5k\Omega$ and $g_m = 11.3$ mA/V .

6. Draw the low frequency equivalent circuit of FET.

7. Find the unit gain bandwidth of MOSFET whose $g_m = 6$ mA/V, $C_{gs} = 8$ pF, $C_{gd} = 4$ pF and $C_{ds} =$ pF.

8. The ac schematic of an NMOS common-source stage is shown in the Figure Q.8, where part of the biasing circuits has been omitted for simplicity. For the N-channel MOSFET M_1, the transconductance, $g_m = 1$ mA/V , and body effect and channel length modulation effect are to be neglected. Find the lower cutoff frequency.

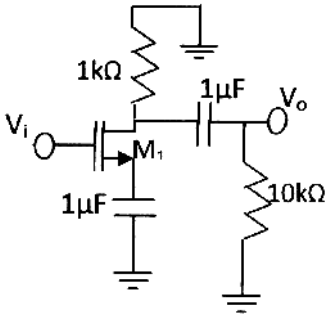

Figure Q.8

9. Mention the different types of active loads.

10. Draw a NMOS current source.

PART B — (5 × 13 = 65 marks)

11. (a) Analyze a BJT with a voltage divider bias circuit, and determine the change in the Q-point with a variation in β when the circuit contains an emitter resistor. Let the biasing resistors be $R_{BI} = 56k\Omega$, $R_{B2} = 12.2k\Omega$, $R_C = 2K\Omega$, $R_E = 0.4k\Omega$, $V_{CC} = 10V$, $V_{EE(ON)} = 0.7V$ and $\beta = 100$.

Or

(b) Consider the circuit shown below in Fig. Q.11(b) with transistor parameters $I_{DSS} = 12\,mA$, $V_P = -4V$, and $\lambda = 0.008\,V^{-1}$. Determine the small-signal voltage gain $A_V = vo/vi$.

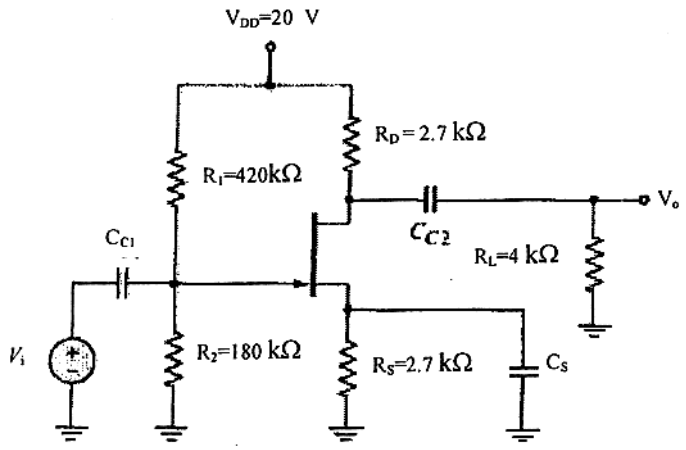

Fig. Q.11(b)

12. (a) Draw the circuit diagram of a Common Emitter amplifier with voltage divider bias, coupling capacitor and bypass capacitor. With the help of small-signal equivalent circuit, obtain the expression for voltage gain, current gain, input and output impedance. (13)

Or

(b) (i) With relevant circuit diagrams, explain the differential amplifier applied with common mode voltage and differential mode voltage. (8)

(ii) Draw the h-parameter model of Common emitter NPN transistor and obtain its h-parameters. (5)

13. (a) Derive gain, input and output impedance of common source JFET amplifier with neat diagram and equivalent circuit. (13)

Or

(b) Draw a common Gate MOSFET amplifier and derive for Av, Ai and Ri using small signal equivalent circuit.

14. (a) (i) For the circuit shown in Figure Q.14(a)(i), let $V_{DD} = V_{SS} = 1.5$ V, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, all channel lengths = 1 μm, $K_n = 200\ \mu\text{A/V}^2$, $K_p = 80\ \mu\text{A/V}^2$ and $\lambda = 0$. For $I_{ref} = 10\ \mu$A, find the widths of all transistors to obtain $I_2 = 60\ \mu$A, $I_3 = 20\ \mu$A and $I_5 = 80\ \mu$A. It is further required that the voltage at the drain of Q_2 be allowed to go down within 0.2 V of the negative supply and voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply. (8)

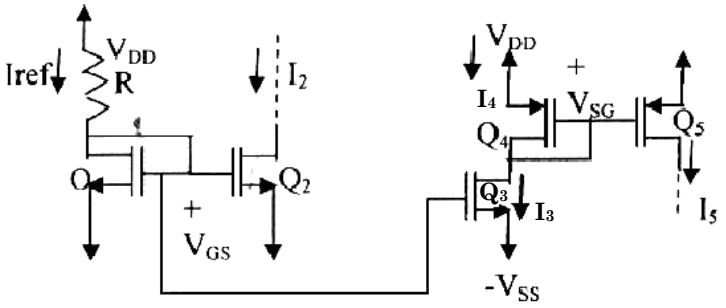

Figure Q.14(a)(i)

(ii) For the NMOS inverter circuit with saturated load (vide Figure Q.14(a)(ii)), the transistor parameters are: (device data for M_D: $V_{tn_D} = 1$ V, $K_{n_D} = \mu_n Cox(W/L) = 100\ \mu\text{A/V}^2$, $\lambda_{n_D=0}$ and device data for M_L: $V_{tn_L} = 1$ V, $K_{n_L} = \mu_n Cox(W/L) = 20\ \mu\text{A/V}^2$ and $\lambda_{n_L} = 0$). Draw its voltage-transfer characteristics curve, and mark down its transition points. (3)

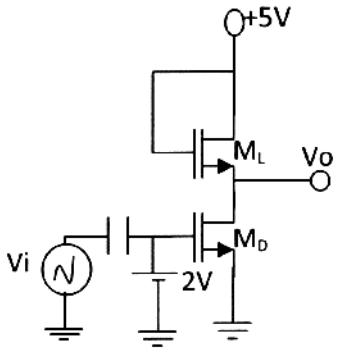

Figure Q.14(a)(ii)

(iii) For CMOS differential amplifier with NMOS differential pair and PMOS current source as active load. Given $I_{DQ} = 500\ \mu A$, $(W/L)_{NMOS} = 5$, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $\lambda_n = 0.01\ V^{-1}$, $\lambda_p = 0.02\ V^{-1}$. Find differential mode voltage gain. (2)

Or

(b) (i) Consider the circuit of NMOS amplifier with depletion load (Vide Figure Q.14(b)(i)). The transistor parameters are $V_{TND} = 0.8\ V$, $V_{TNL} = -1.2\ V$, $\beta_{nD} = (\mu_{nD} C_{ox}(W/L)) = 500\ \mu A/V^2$, $\beta_{nL} = (\mu_{nD} Cox(W/L)) = 50\ \mu A/V^2$, $I_{DQ} = 100\ \mu A$, $V_{DD} = 5\ V$ and $\lambda_{nD} = \lambda_{nL} = 0.01\ V^{-1}$. (1) Determine V_{GS} such that the Q-point is the mid of the saturation region. (2) Calculate Q-point drain current. (3) Determine the small signal voltage gain. (6)

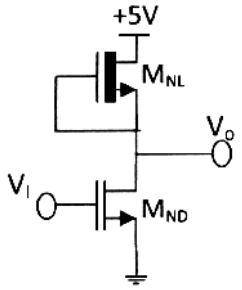

Figure Q.14(b)(i)

(ii) Determine the voltage gain, input impedance, output impedance of CMOS source follower amplifier. (7)

15. (a) Discuss the operation of MOS differential Amplifier with active and derive for CMRR.

Or

(b) Explain in detail the operation of CMOS common source and source follower with neat diagram and derive for Av.

PART C — (1 × 15 = 15 marks)

16. (a) Find the Midband gain A_M and upper 3 — dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance R_{sig} = 100 $K\Omega$. The Amplifier has RG = 4.7 MΩ, R_D = R_L =15 KΩ, g_m=1 mA/V, r_0=150 KΩ ,C_{gs} = 1pF and C_{gd} = 0.4pF. (15)

Or

(b) Calculate the input and output resistance of the emitter- follower circuit shown in Fig. Q.16(b). Assume $R_s = 0.5\ k, r\pi = 3.28\ K\Omega, \beta = 100$ and $r_0 = 100\ K\Omega$.

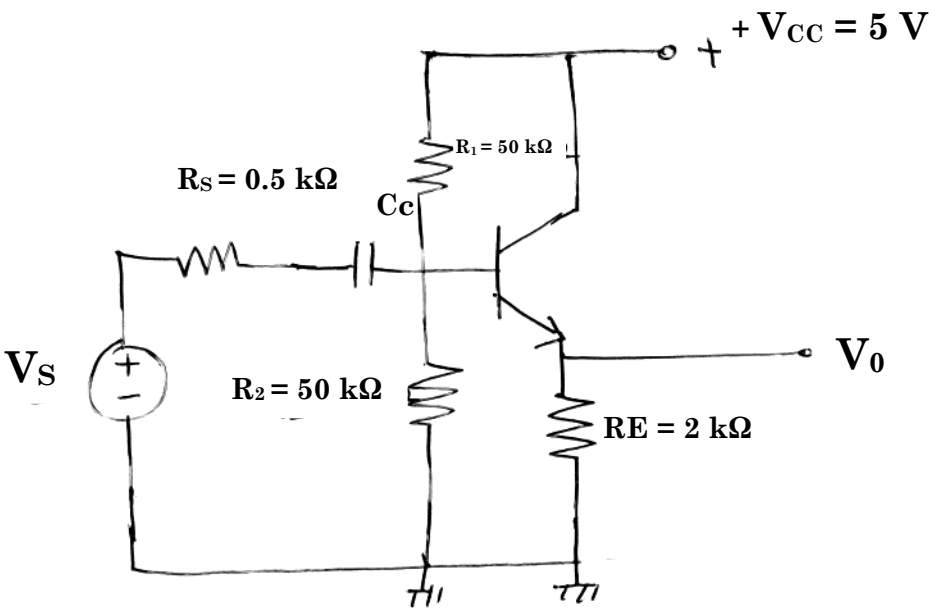

Fig. Q.16 (b)